Performance Evaluation of the HI5746 Using the HI5703 Evaluation Board

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For the most updated information see Application Note AN9725 (HI5746EVAL)

Description

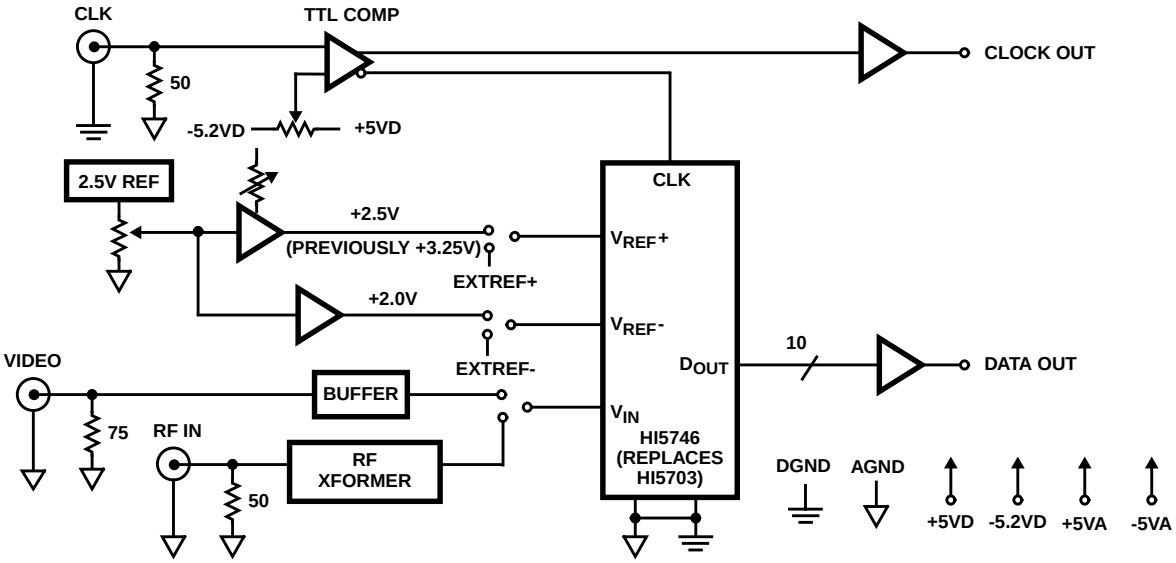
The HI5703EVAL evaluation board can be used to evaluate the performance of the HI5746 10-bit 40 MSPS analog-to-digital converter (ADC). The HI5703EVAL evaluation board is made electrically compliant with the HI5746 by making a simple resistor change in the reference voltage generation circuits allowing the former +3.25V reference generator circuit to be adjustable to +2.5V.

As shown in the HI5703EVAL Evaluation Board (Modified) Block Diagram, the evaluation board includes clock driver circuitry, reference voltage generators (modified), and a choice of analog input drive circuits. Buffered digital data outputs are conveniently provided for easy interfacing to a ribbon connector or logic probes. The evaluation board is provided with some prototyping area for the addition of user designed custom interfaces or circuits. Additionally, the evaluation board is provided with eight removable jumpers to allow for various operational configurations. Refer to AN9534, “Using the HI5703 Evaluation Board”, for a complete technical discussion on the evaluation board.

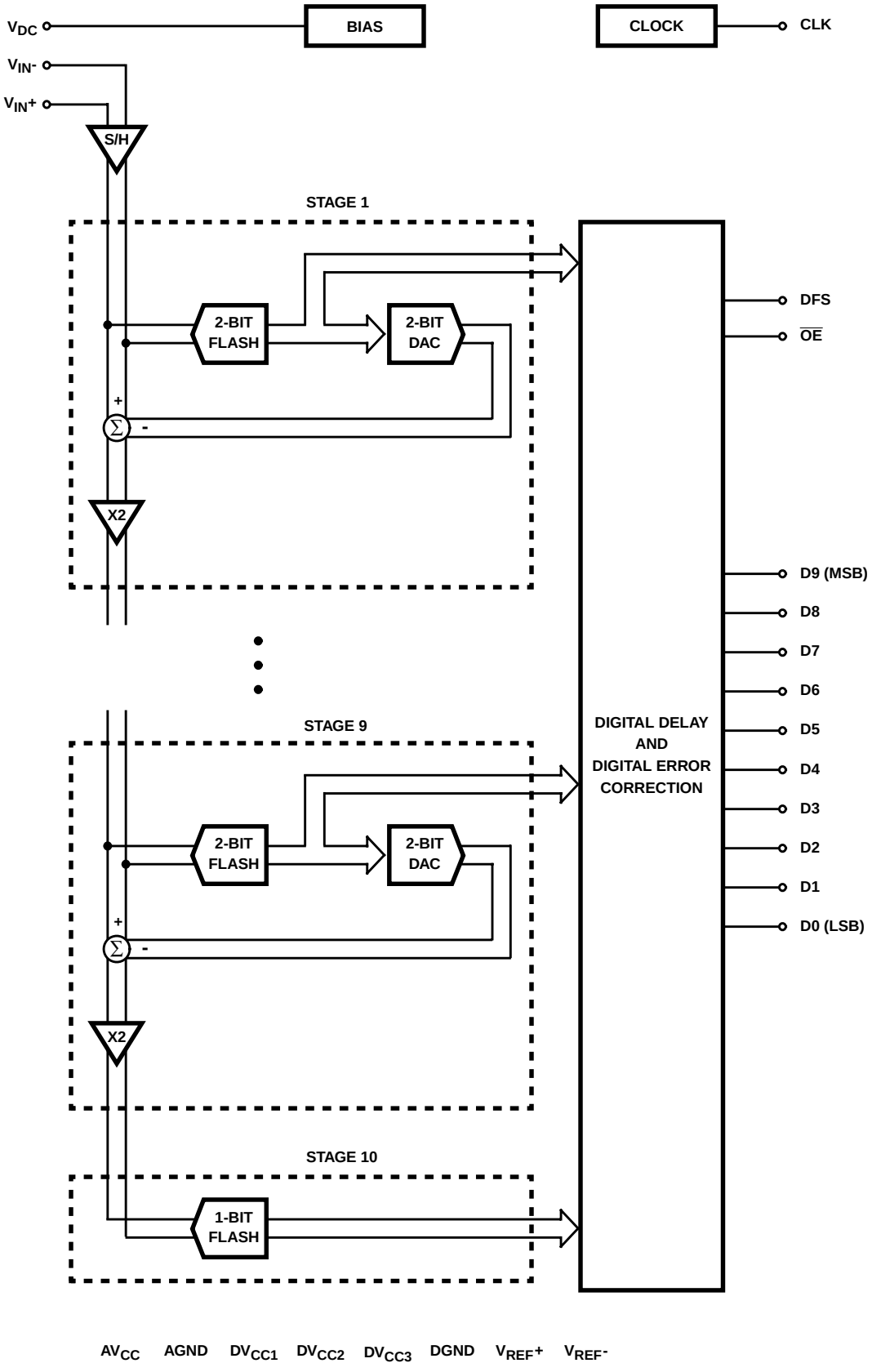
HI5746 A/D Theory of Operation

The HI5746 is a 10-bit fully differential sampling pipelined A/D converter with digital error correction. Figure 1 depicts the circuit for the converters front-end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, $\phi 1$ and $\phi 2$, derived from the master clock (CLK) driving the converter. During the sampling phase, $\phi 1$, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of $\phi 1$ the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, $\phi 2$, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op amp output nodes. The charge then redistributes between C_S and C_H, completing one sample-and-hold cycle. The output of the sample-and-hold is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function, but can also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of the switches and C_S. The relatively small values of these components result in a typical full power input bandwidth of 100MHz for the HI5746 converter.

HI5703EVAL Evaluation Board (Modified) Block Diagram



HI5746 Functional Block Diagram



As illustrated in the HI5746 Functional Block Diagram and the timing diagram in Figure 2, nine identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the front end S/H circuit with the tenth stage being a one-bit flash converter. Each converter stage in the pipeline will be sampling in one clock phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal so that alternate stages in the pipeline will perform the same operation.

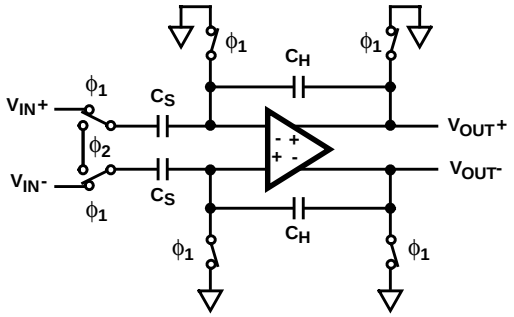
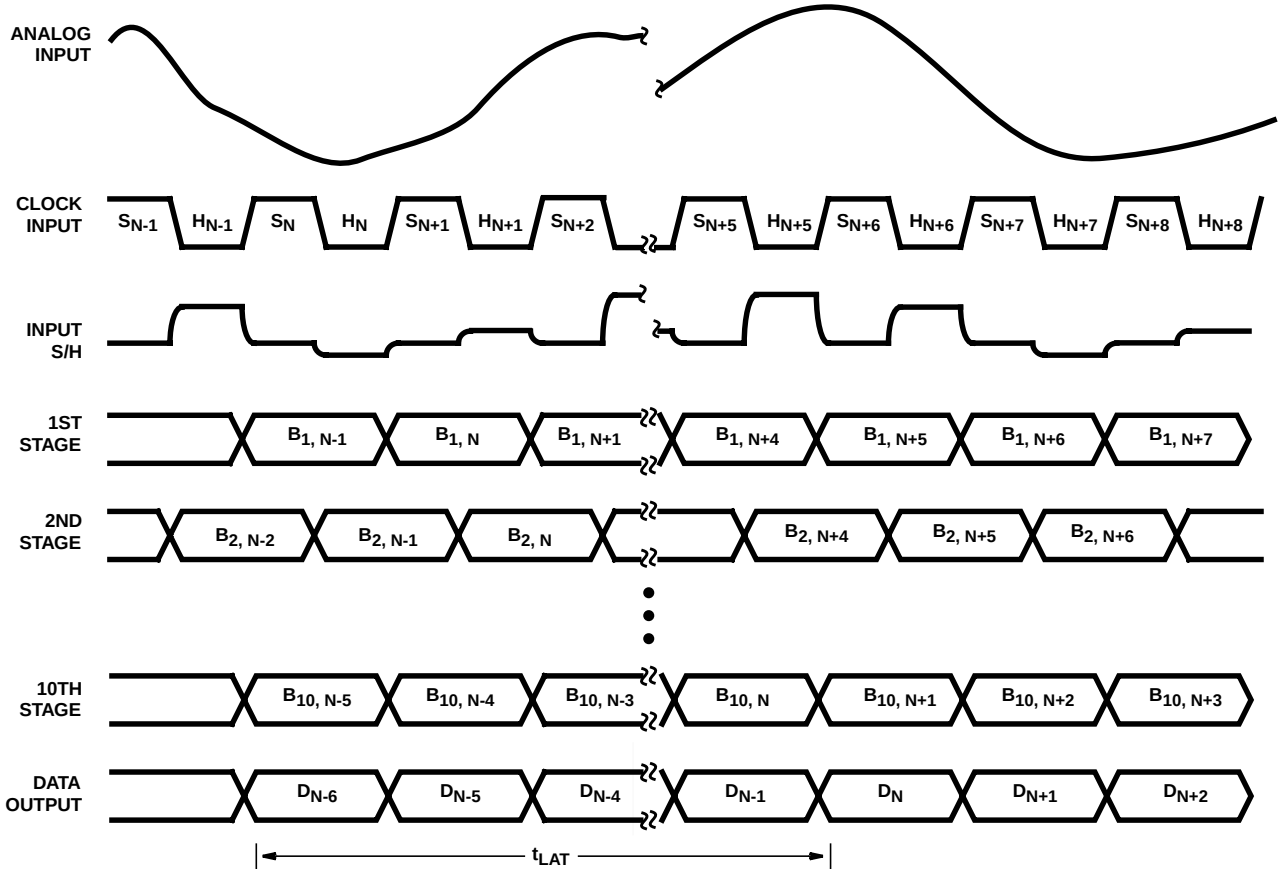


FIGURE 1. ANALOG INPUT SAMPLE-AND-HOLD

The output of each of the nine identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal clock. The function of the digital delay line is to time align the digital outputs of the nine identical two-bit subconverter stages with the corresponding output of the tenth stage flash converter before inputting the nineteen-bit result into the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten-bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output on the bus at the 7th cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a double buffered latching technique. The output of the digital correction circuit is available in two's complement or offset binary format depending on the condition of the Data Format Select (DFS) input.



NOTES:

1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 2. HI5746 INTERNAL CIRCUIT TIMING

Reference Voltage Generator Circuit and Modifications

The HI5746 A/D contains a resistive voltage divider between the V_{REF}+ reference voltage input pin and analog ground. The divider tap is brought out to the V_{REF}- reference voltage input pin. The A/D requires one reference voltage connected to the V_{REF}+ input pin with the other, optional, reference voltage connected to the V_{REF}- input pin. The reference voltage that drives V_{REF}+ must be able to source the maximum reference current, 1mA. The reference voltage that drives V_{REF}- has minimal current drive requirements, typically <100µA. The HI5746 is tested with V_{REF}- equal to 2V and V_{REF}+ equal to 2.5V for a fully differential analog input voltage range of ±0.5V.

In order to make the HI5703EVAL evaluation board electrically compliant with the HI5746 it is necessary to change the value of one resistor in the V_{REF}+ reference voltage generator. All that is required is to change R16 from 15kΩ to 10kΩ, refer to the evaluation board parts layout (Figure 3) and the schematics for the location of R16. This change in resistance value will allow adjustment of the V_{REF}+ reference voltage generator output from +2.2V to +3.4V thus allowing for testing of the HI5703 or HI5746.

The reference circuit on the HI5703EVAL evaluation board contains a precision +2.5V reference (U4) along with operational amplifiers (U5A and U5B) that are utilized to generate the reference voltages for the HI5746. After the required modification to the value of resistor R16 the reference voltages are set to the levels required by the HI5746 as follows. The V_{REF}- reference input is set **FIRST** by monitoring JP6 with a DVM and adjusting R11 until a reading of 2.0V ±5mV is obtained. Next the V_{REF}+ reference input is set by monitoring JP5 with a DVM and adjusting R15 until a reading of 2.5V ±5mV is obtained.

The reference voltages are connected to the HI5746 through the use of jumpers. Jumper JP5 is used to connect the +2.5V reference voltage and jumper JP6 is used to connect the +2.0V reference voltage.

It should be noted that operation of the HI5746 with a single +2.5V voltage reference can be demonstrated by simply removing jumper JP6 thereby removing the +2.0V V_{REF}- reference voltage from the converter.

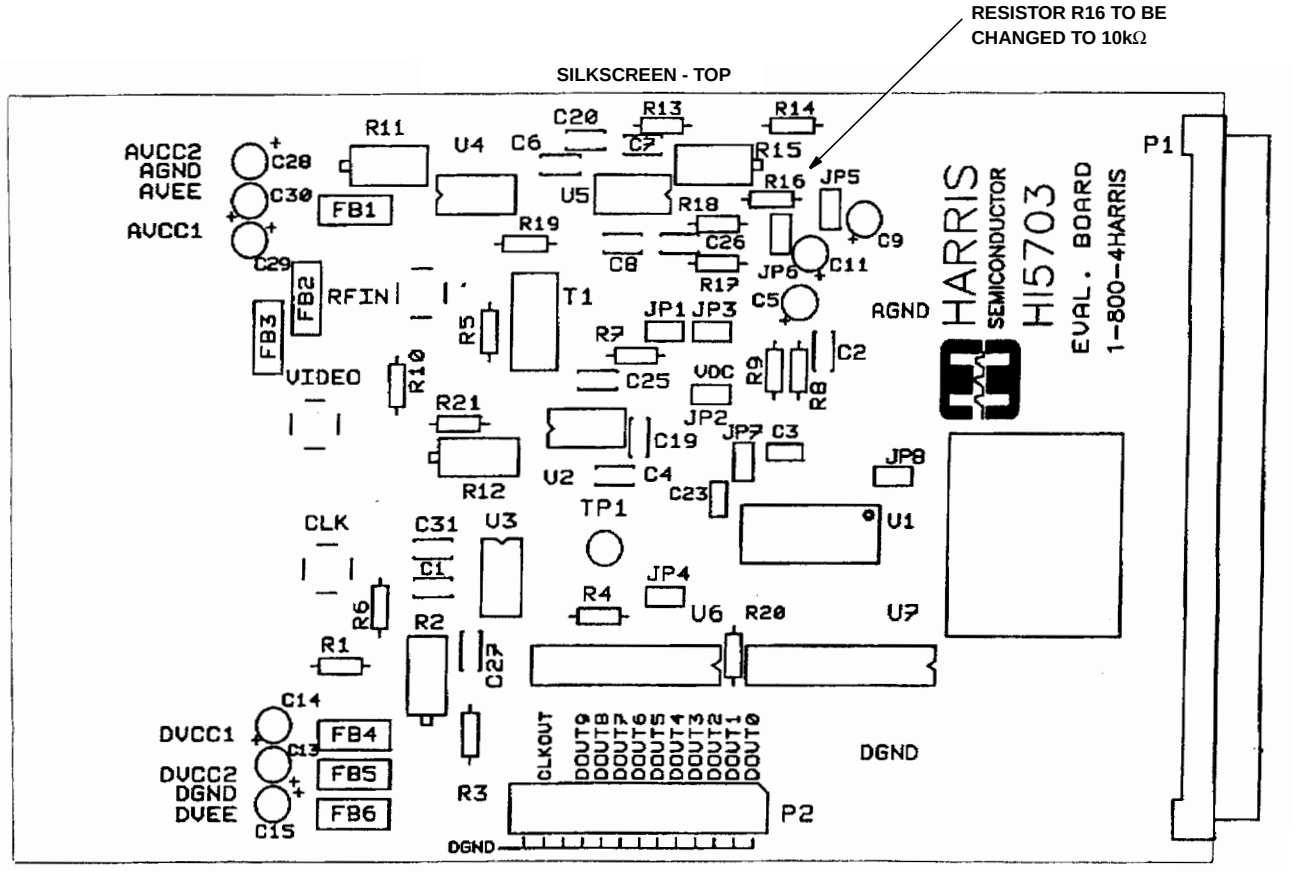
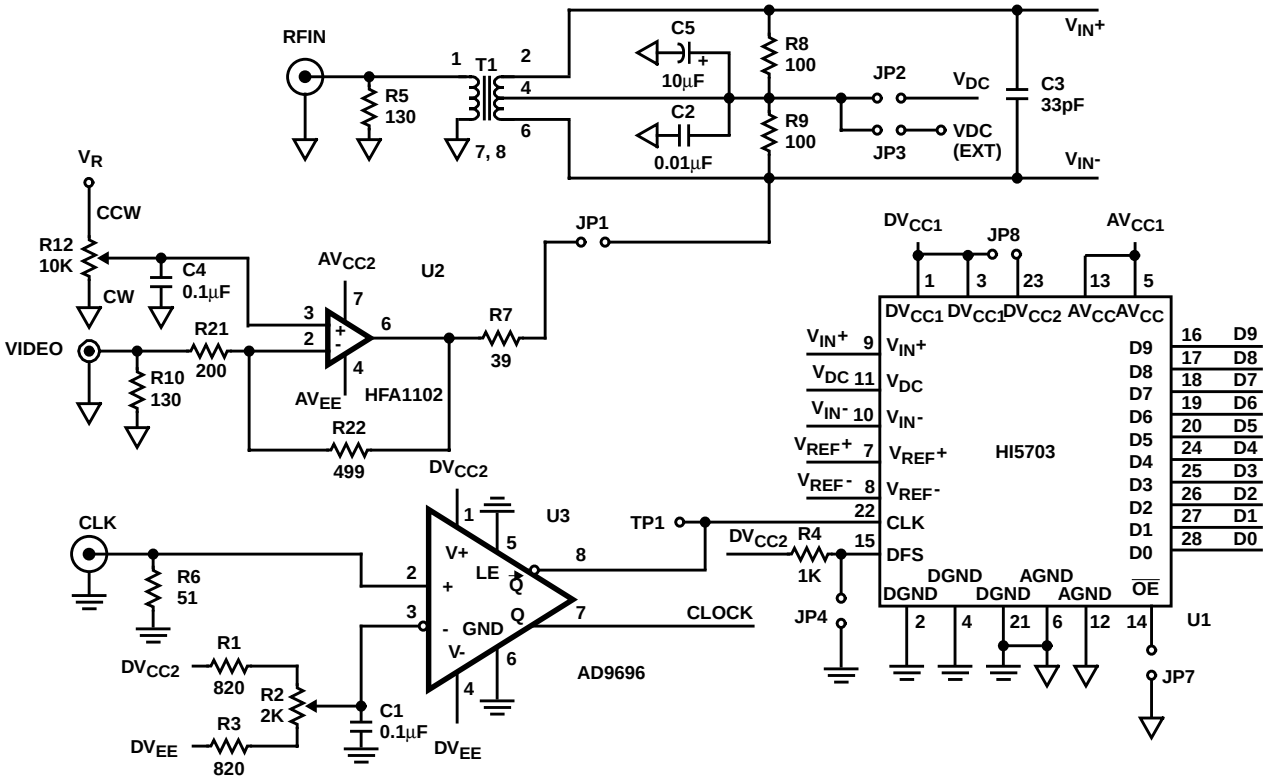
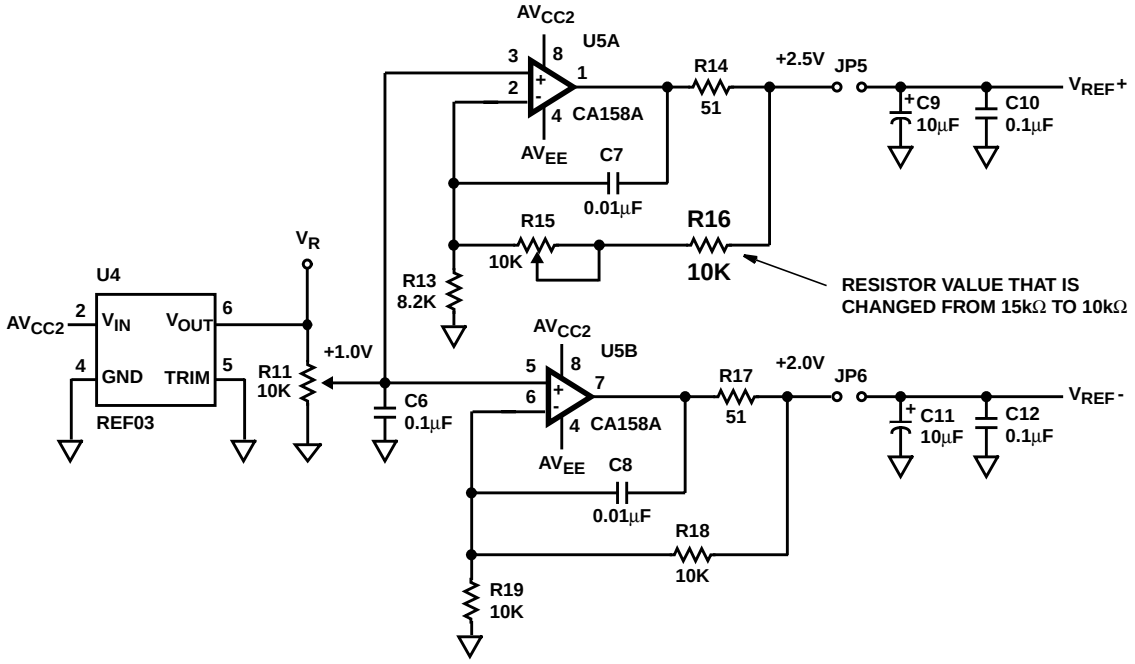


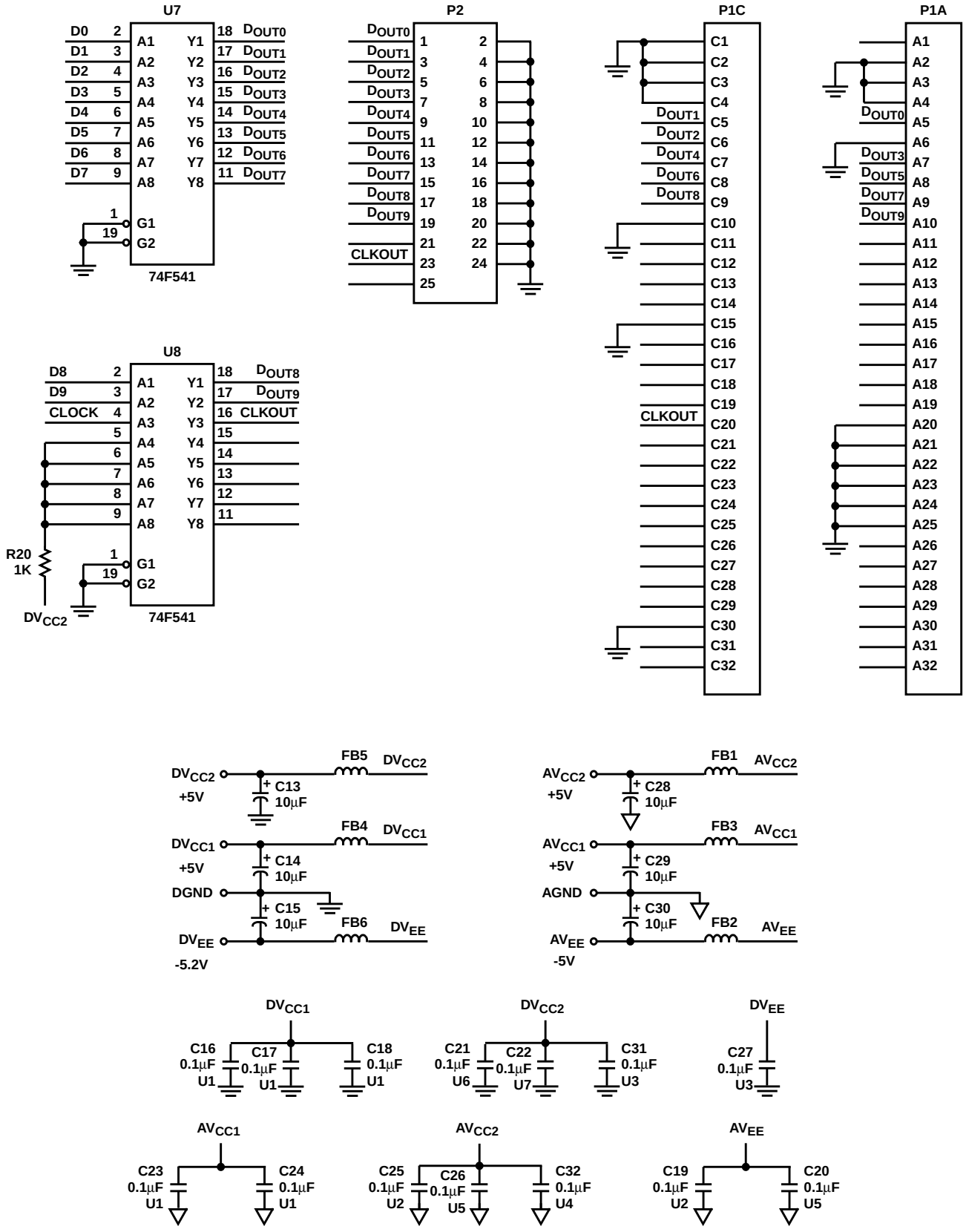
FIGURE 3. HI5703EVAL EVALUATION BOARD GROUND LAYER

HI5703EVAL Evaluation Board Schematic Diagrams





HI5703EVAL Evaluation Board Schematic Diagrams (Continued)



HI5703EVAL Evaluation Board Parts List

REFERENCE DESIGNATOR	QTY	DESCRIPTION
R4, R20	2	1kΩ, 1/8W, 5%
R1, R3	2	820Ω, 1/8W, 5%
R6, R14, R17	3	51Ω, 1/8W, 5%
R18, R19	2	10kΩ, 1/8W, 5%
R8, R9	2	100Ω, 1/8W, 5%
R7	1	39Ω, 1/8W, 5%
R21	1	200Ω, 1/8W, 5%
R16	1	10kΩ, 1/8W, 5% (previously 15K)
R13	1	8.2kΩ, 1/8W, 5%
R5, R10	2	130Ω, 1/4W, 5%
R22	1	499Ω, 1206 CHIP
R2	1	2kΩ Trim Pot
R12, R11, R15	3	10kΩ Trim Pot
C5, C9, C11, C13, C14, C15, C19, C25, C28, C29, C30	11	10µF Tant Cap, 35WVDC, 20%
C2, C7, C8	3	0.01µF Ceramic Cap, 100WVDC, 10%
C33, C34	2	1000pF 1206 Chip Cap, 50WVDC, XR7 10%
C1, C4, C6, C20, C26, C27, C31	7	0.1µF Ceramic Cap, 50WVDC, 10%
C10, C12, C16, C17, C18, C21, C22, C23, C24, C32	10	0.1µF 1206 Chip Cap, 50WVDC, Z5U, 20%
C3	1	33pF 1206 Chip Cap, 100WVDC, COG(NPO), 5%
FB1-6	6	10µH Ferrite Bead
T1	1	RF Transformer
TP1	1	Probe Tip Adapter
JP1-8	8	1 x 2 Header
J1-8	8	1 x 2 Header Jumper
P2	1	2 x 13 Header
VDC, AGND, DGND	3	Test Point
P1	1	64-Lead DIN RT Angle
SMA1-3	3	SMA, Straight Female Jack PCB MNT
SU2-5, ST1	5	8-Lead Socket
SU6-7	2	20-Lead Socket
U1	1	Intersil HI5703KCB 10-Bit 40MHz A/D Converter
U2	1	Intersil HFA1102IP Operational Amplifier
U3	1	Ultrafast Voltage Comparator
U4	1	+2.5V Precision Voltage Reference
U5	1	Intersil CA158AE Operational Amplifier
U6-7	2	Octal Buffer/Line Driver